The demand for breakthrough performance has driven integration technology to new levels of complexity in semiconductor package designs. The need for compact, high performance semiconductor packages is challenging traditional packaging technology in the areas of form factor, reliability and performance. Integration is increasingly moving from substrate-based package con□gurations to wafer level package designs.

As die sizes and lithography nodes shrink, the JCET Group of companies is driving a number of integration solutions in wafer level packaging, including Fan-in Wafer Level Packaging (FIWLP), Fan-out Wafer Level Packaging (FOWLP), System-in-Package (SiP), Ultra Finem[.7.4Lrch Or (stgs dc S (a)4 (t)6 (e)-27.9), uFOSrAs need ugh pery□gulaVttegrtion sol6.1 (dack)-18sen proven reliability and design □exibility, we o□er a full range of advanced wafer level technology solutions to help you meet your business goals.

Fan-in WLP: Compact Packaging Solution

As a small, lightweight, high performance semiconductor solution, Wafer Level Chip Scale Packaging (WLCSP) is a Fan-in wafer level package (WLP) that o□ers compelling advantages for cost and space constrained mobile devices and new applications such as wearables and automotive electronics.

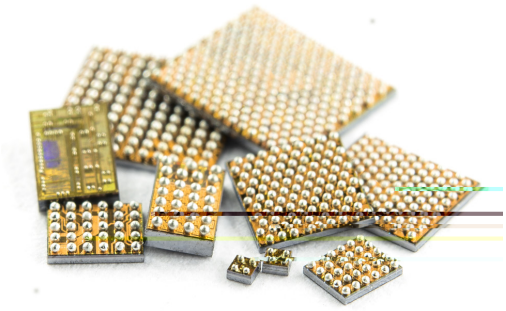
With WLCSP, all of the manufacturing process steps are performed in parallel at the silicon wafer level rather than sequentially on individual chips to achieve a package that is essentially the same size as the die.

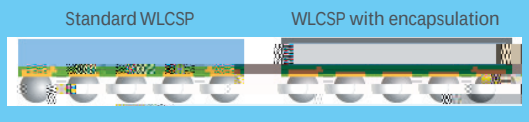
The basic structure of WLCSP comprises an active surface with polymer coatings and bumps with bare silicon (Si) exposed on the remaining sides. The WLCSP provides the smallest possible package size since the □nal package is no larger than the die itself. WLCSP solutions provide signi□cant package footprint reductions, lower cost, improved electrical performance, and a relatively simpler construction over conventional wirebond or interposer packaging technologies.

The volume of WLCSP packages used in the industry has experienced steady growth driven by the small form factor and high performance requirements of mobile and consumer products.

Encapsulation for Increased Reliability

Since WLCSP is essentially a bare die with exposed Si surfaces, there is always risk the package may su□er mechanical damage in the form of chipping and cracking





eWLCSP™ and FI-ECP

We o□er two types of Fan-in WLP with protective sidewall coating – encapsulated Wafer Level Chip Scale Packaging (eWLCSP) and Fan-in Encapsulated Chip Package (FI-ECP).

With eWLCSP, the formation of a protective polymer coating on the back and four sides of the die surfaces is accomplished using the same high volume reconstitution and wafer level molding process that is used for our Fan-out embedded Wafer Level Ball Grid Array (eWLB) technology.

eWLB

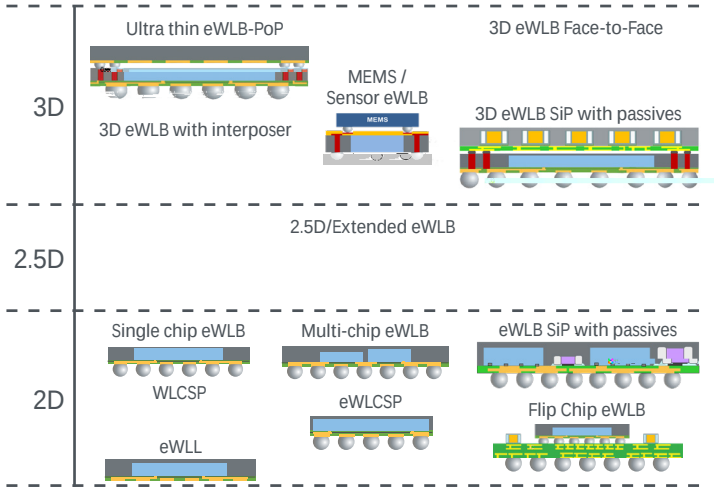
Embedded Wafer Level Ball Grid Array (eWLB) is one of the most widely adopted FOWLP solutions in the semiconductor industry today. eWLB provides a signi□cant increase in routing density combined with an unparalleled reduction in package size and thickness which is not attainable with substrate-based packages. The smaller form factor helps to free up space on the circuit board. The short interconnection lengths combined with thinner dielectric materials also produce better electrical performance with a signi□cant reduction in power consumption, thereby improving battery life.

JCET, was one of the □rst companies to ramp eWLB to high volume production over 9 years ago and has driven a number of industry-wide technology achievements such as dense vertical interconnections as high as 500 – 1,000 I/O, very □ne line and widths spacing down to 2 m/2 m, ultra-

2.5D / 3D eWLB Integration

The integration capabilities and design □exibility of eWLB is driving adoption in a number of emerging market segments such as Internet of Thigns (IoT), wearable electronics such as health bands and cardiac monitoring devices, □ngerprint sensors, MEMS, 5G mmWave devices, and automotive applications such as Advanced Driver Assistance Systems (ADAS). If the end application requires a reduction in form factor and thinner package with a high level of integration and robust reliability, eWLB can provide a superior solution.

Our extensive eWLB portfolio includes small die, large die, side-by-side multi-die, MEMS, 2.5D and 3D Package-on-Package (PoP) and System-in-Package (SiP) architectures.



Fan-out Encapsulated Chip Package

FO-ECP

Through Silicon Via (TSV)

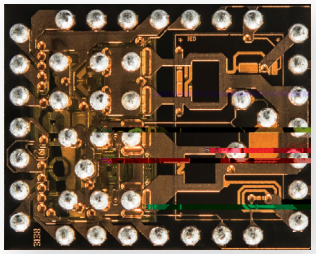
Through Silicon Via (TSV) utilizes short vertical interconnections or “vias” that pass through a silicon wafer in order to achieve greater space e□ciencies and higher interconnect densities than wire bonding and □ip chip stacking. When combined with microbump bonding and advanced □ip chip technology, TSV technology provides the ability to scale semiconductor devices to smaller and smaller geometries with higher input/output.

We understand the cost and supply chain limitations our customers face with utilizing TSV technology. The JCET Group is focused on providing customers with cost e□ective TSV solutions in key areas.

For over two years JCET has been in volume production of 3D TSV for 200mm CMOS Image Sensor (CIS) wafers. The tapered via utilizes a via-last approach to contact the die pad from the wafer backside. This proven approach is also a good □t for other sensor applications such as □ngerprint sensors (FPS) or pressure sensors.

For 3D integrated circuits, JCET has a full front- to back-end manufacturing capabilities and currently handles both chip-to-chip (C2C) and chip-to-wafer (C2W) assembly for 3D TSV technology. This includes high density microbump capabilities in both solder and copper column, microbump bonding down to 40 m pitch, thin wafer handling, wafer-level under□ll, thin wafer dicing and microbumps for □ip chip interconnection. Microbump technology is critical to delivering □ne pitch, low pro□le solutions for high performance devices.

Integrated Passive Devices (IPD)



Passive devices such as resistors, capacitors, inductors, □lters and baluns can consume 60-70% of available space in a system, subsystem or SiP. As one of the □rst companies in the industry to integrate and fabricate passive devices at the silicon wafer level, we are able to produce IPDs which are signi□cantly smaller, thinner and higher performing than standard discrete passive devices that are commercially available today.

With this knowledge and experience, we have embeded passive devices in very close proximity to the active die, providing signi□cant performance, size reduction and device integration in SiP con□gurations that address 2.5D and 3D integration requirements.

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